METHODS OF ROUTING PROGRAMMABLE LOGIC DEVICES TO MINIMIZE PROGRAMMING TIME

ABSTRACT

Methods of routing a design in a programmable logic device (PLD) to increase the effectiveness of applying a multi-frame write (MFW) compression technique to the resulting configuration bitstream. The methods apply placement patterns and/or routing templates to encourage the inclusion of numbers of duplicated routing paths in the routed design. The duplicated routing paths result in duplicated configuration data. Thus, a configuration bitstream implementing the routed design in the PLD includes numbers of duplicated configuration data frames, and is well-suited to benefit from MFW compression techniques.